

FORM PTO-1449 (Modified)  
U.S. Department of Commerce, Patent and Trademark Office

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)

Docket No.

99-039

Serial No.

Applicants

Sheldon Aronowitz et al.

Filing Date  
Herewith

Group

U.S. PTO  
09/464297

12/15/99

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
C.B.	AA	5,874,367	2/23/99	Dobson	438	787	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

Translation

		Document Number	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

C.B.	AR	Bothra, S., et al., "Integration of 0.25 $\mu$ m Three and Five Level Inter-connect System for High Performance ASIC", <u>1997 Proceedings Fourteenth International VMIC Conference</u> , Santa Clara, CA, June 10-12, 1997, pp.43-48.
C.B.	AS	Dobson, C.D., et al., "Advanced SiO <sub>2</sub> Planarization Using Silane and H <sub>2</sub> O <sub>2</sub> ", <u>Semiconductor International</u> , December 1994, pp. 85-88.
C.B.	AT	McClatchie, S., et al., "Low Dielectric Constant Oxide Films Deposited Using CVD Techniques", <u>1998 Proceedings Fourth International DUMIC Conference</u> , February 16-17, 1998, pp. 311-318.

Examiner

Chaulett C Brog

Date Considered

5-31-01

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

CB	AR	Peters, Laura, "Pursuing the Perfect Low-k Dielectric", <u>Semiconductor International</u> , Vol. 21, No. 10, September, 1998, pp. 64-66, 68, 70, 72, and 74.
	AS	
	AT	

Examiner

*Chen-Lott*

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